APPENDIX A - CLEAN COPY OF PENDING CLAIMS

1. (Twice Amended) A semiconductor package, comprising:

a semiconductor chip provided with a plurality of input/output pads on its upper surface;

a chip paddle adjacent a bottom surface of the semiconductor chip, said chip paddle having an upper surface;

a plurality of internal leads surrounding the chip paddle wherein the upper surface of the chip paddle and at least one portion of an upper surface of the internal leads are in approximately a common plane, and wherein the chip paddle is in at least one part thicker than at least a portion of the internal leads;

conductive wires for electrically connecting the input/output pads of the semiconductor chip to the internal leads; and

a package body comprised of encapsulation material that encapsulates the semiconductor chip, the conductive wires, the chip paddle and the internal leads, wherein the chip paddle and the internal leads are externally exposed at a bottom surface of the chip paddle and the internal leads.

4. The semiconductor package as set forth in claim 1, wherein:

the chip paddle and a lower surface of the internal leads are in a common plane, and wherein the chip paddle is thicker than the internal leads.

5. The semiconductor package as set forth in claim 1, wherein:

the chip paddle is bonded to a bottom surface of the semiconductor chip with an adhesive.

6. The semiconductor package as set forth in claim 1, wherein:

each of the internal leads have an etched part at an end facing the chip paddle.

7. The semiconductor package as set forth in claim 1, wherein:

the internal leads are externally exposed at their side surfaces and bottom surfaces.

13. (Twice Amended) A packaged semiconductor, comprising:

a chip paddle adapted to receive a semiconductor chip, said chip paddle having an upper surface, a lower surface, and an intermediate surface positioned between and parallel to the upper surface and the lower surface;

a plurality of internal leads surrounding the chip paddle wherein the chip paddle and the leads comprise a leadframe wherein the intermediate surface of the chip paddle and at least one portion of an upper surface of the internal leads are in approximately a common plane, and wherein the chip paddle is at least one part thicker than at least a portion of the internal leads; and

the leadframe adapted to receive a package body comprised of encapsulation material for encapsulating the chip paddle and the internal leads, wherein the chip paddle and the

internal leads are externally exposed at a bottom surface of the chip paddle and the internal leads.

14. The packaged semiconductor as set forth in claim 13, wherein:

a lower side area of the chip paddle has an etched part wherein the etched part is about 10% to about 90 % of the lower side area of the chip paddle, and the etched part is located inside the package body.

17. The packaged semiconductor as set forth in claim 13, wherein:

each of the internal leads have an etched part at an end facing the chip paddle.

18. The packaged semiconductor as set forth in claim 13, wherein:

the internal leads are externally exposed at their side surfaces and bottom surfaces.

19. (Amended) A package for mounting a semiconductor chip, comprising:

a leadframe, the leadframe comprising;

a chip paddle wherein a surface of the chip paddle is externally exposed from the package; and

a plurality of internal leads surrounding the chip paddle, wherein a surface of each of the plurality of internal leads is externally exposed from the package;

means for receiving encapsulating material for encapsulating the leadframe;

means for locking the encapsulating means to the chip paddle;

means for providing a fluid path for the encapsulating means during encapsulation of the leadframe; and

said means for locking and said means for providing a fluid path are formed from a void caused by said chip paddle being in at least one part thicker than at least a portion of the internal leads.

20. The package as set forth in claim 19, wherein the chip paddle has an etched portion on a lower side area of the chip paddle.

21. The package as set forth in claim 20, wherein the etched portion is about 10% to about 90% of the lower side area of the chip paddle.

22. The package as set forth in claim 21, wherein the means for locking comprises the etched portion.

23. The package as set forth in claim 21, wherein the means for providing a fluid path comprises the etched portion.

25. (Amended) The package as set forth in claim 21, wherein the etched portion is located inside the package body, an upper surface of the chip paddle and a lower surface of the plurality of internal leads are in approximately a common plane, the chip paddle is bonded to a bottom surface of a semiconductor chip and at least one of the plurality of internal leads has an etched part at an end facing the chip paddle.